Remarks:

Reconsideration of the application is requested.

Claims 1-16 remain in the application. Claims 1, 8 and 11 have been amended. Claims 13-16 have been withdrawn from consideration.

In item 2 on page 2 of the above-identified Office action, claim 8 has been objected to because of an informality. Appropriate correction has been made.

In item 4 on pages 2-3 of the above-mentioned Office action, claims 1, 6, 10 and 11 have been rejected as being anticipated by Hsu et al. (US Pat. No. 6,011,285) under 35 U.S.C. § 102(e).

The rejection has been noted and claims 1 and 11 have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 3, lines 21-22 of the specification.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claims 1 and 11 call for, inter alia:

a diode structure connecting said first gate electrode to said second gate electrode.

Hsu et al. describe a c-axis oriented thin film ferroelectric transistor memory cell. This memory cell has a so-called FEM-stack 48 including a lower electrode 50 made of Pt, Ir, IrO_2, or an alloy of Pt/Ir, a ferroelectric layer 52, and an upper electrode 54 made of the same material as the lower electrode (see column 5, lines 9 - 30 and Fig. 4).

In another embodiment, Hsu et al. disclose a two transistor memory cell having a MOS transistor 82 and a FEM gate unit 48. The MOS transistor 82 includes a gate stack formed by a SiO_2 layer 88 serving as gate dielectric, and a polysilicon layer 90 covered by a silicide layer 92 which together form a gate electrode. This gate stack is covered by a SiO_2 layer 94 (see column 8, lines 37 - 59). The gate unit 48 includes a lower electrode 50, a ferroclectric layer 52, and an upper electrode 54 (see column 8, lines 60 - 67). Again, lower and upper electrode 50, 54 are made of the same materials as described with respect to Fig. 4 (see column 8, lines 65 - 66: "lower electrode 50 may beformed as previously described"; column 9, lines 4 - 5: "The upper electrode may be formed of the same materials as the lower electrode"). Fig. 8 and the accompanying description of Hsu et al. leave it open as to whether and how

the gate electrode 90 of the MOS-stack 82 and the upper electrode 54 of the FEM gate unit 48 are connected with each other. Fig. 8 suggests that there is no connection between the gate electrode 90 and lower electrode 50 or upper electrode 54, since the gate electrode 90 or the silicide layer 92 is completely covered by an insulating SiO_2 layer 94 (see column 8, lines 45 - 59 and Fig. 8).

In yet another embodiment, to which the Examiner refers, a MFMOS memory cell "includes a c-axis oriented, ferroelectric (FE) capacitor, or FEM gate unit, located on top of a MOS capacitor" (see column 16, lines 30 - 32). This structure is described in more detail in column 16, line 54 to column 17, line 33 and is depicted in Fig. 12 of Hsu et al.

An oxide layer 124 is formed on the surface of a silicon substrate 80 having a p^- well 122. An optional n^+-polysilicon layer 126, a lower electrode 50, a ferroelectric layer 52, and an upper electrode 54 are deposited onto this layer. Together they form a FEM gate unit or FEM capacitor 48 (see column 17, lines 15 - 21). The nature of the inverted U-shaped structure in Fig. 12 which covers the upper and lower electrode 54, 50 and the ferroelectric layer 52 is not described by Hsu et al. It is assumed that this is a TiO_2-layer protecting the ferroelectric

layer. According to column 17, lines 19 - 30 of Hsu et al., after forming the stacked gate unit 48 "a layer of insulating material, such as TiO_x 62" is deposited. In a following step, n^+ source and drain regions 42, 46 are formed. Since regions 42, 46 are aligned with the outer edges of the inverted U-shaped structure, it is believed that this structure must be indeed the TiO_x-layer. Although the TiO_x-layer is referred to as layer 62, this is wrong because in lines 28 - 29 of column 17 a further insulating layer 62 is mentioned which covers the complete structure (see Fig. 12). Therefore, it seems reasonable that the inverted U-shaped structure is made of TiO_2.

However, neither from Fig. 12 nor from the description of Hsu et al. can an electrical connection between a first and a second gate electrode be inferred. For instance, if one assumes that the upper electrode 54 and the lower electrode 50 might be regarded as the first and second gate electrodes, these two electrodes are electrically insulated from each other by the ferroelectric layer 52. This coincides with the wording of Hsu et al. which calls the FEM gate stack a FEM capacitor (see column 17, lines 20 - 21).

On the other hand, if the n^+-polysilicon layer 126 and the lower electrode 50 are regarded as the first and second electrodes,

both layers may be in contact with each other, but these layers do not serve as the first and second gate electrode. From a technical point of view, a gate electrode is a conductive layer which is disposed from the surface of a conductive channel by a gate dielectric layer. The gate electrode controls the electrical current flowing through that conductive channel. With reference to Fig. 12 of Hsu et al., both the n^+-polysilicon layer 126 and the lower electrode 50 are disposed over a conductive channel (p^--well 122) by a SiO_2-layer 124. However the ferroelectric layer 52 is placed over the lower electrode 50. Naturally, the upper electrode 54 cannot be regarded as a conductive channel to be controlled by the lower electrode 50. In contrast to this, claims 1 and 11 of the instant application recite a first and a second gate intermediate layer, whereby the first gate intermediate layer has at least one ferroelectric layer.

Even if one considers the n^+-polysilicon layer 126 and the upper electrode 54 as the first and second gate electrodes, there is no electrical connection between these two layers.

Clearly, Hsu et al. do not show "a diode structure connecting said first gate electrode to said second gate electrode", as recited in claims 1 and 11 of the instant application.

Claims 1 and 11 are, therefore, believed to be patentable over Hsu et al. and since claims 6 and 10 are dependent on claim 1, they are believed to be patentable as well.

In item 5 on pages 3-4 of the above-mentioned Office action, claims 1, 3 and 8 have been rejected as being anticipated by Argos et al. (European Publication No. 0 540 993 A1) under 35 U.S.C. § 102(b).

Argos et al. describe a MOS field effect transistor using a buffer layer / ferroelectric / buffer layer stack as a gate dielectric. Fig. 9 of Argos et al. shows a substrate 10, a first buffer layer 20, a ferroelectric layer 30, a second buffer layer 40, and a gate electrode 50. The gate electrode 50 is in contact with a metallization layer 100 (see column 5, line 15). The gate stack is isolated from those parts of the metallization layer 100 which contact the source and drain regions 60, 70 by an insulating layer 80. It seems that the Examiner considers this insulating layer 80 as a second gate intermediate layer and the metallization 100 as a second gate electrode.

However, it is the understanding of Applicants that a person skilled in the art would not consider the metallization 100 as a

gate electrode. With respect to the remarks given above in conjunction with Fig. 12 of Hsu et al., a gate electrode is disposed from a conductive channel by a gate dielectric and controls the electrical current of that conductive channel. The only conductive channel disclosed by Argos et al. is the substrate region extending between the source and drain regions 60 and 70. However, this conductive channel is covered only by the ferroelectric stack including the buffer layers 20 and 40, and the ferroelectric layer 30. In this configuration shown in Fig. 9 of Argos et al., the metallization layer 100 functions only as an intermetallic contact and not as a gate electrode. The insulating layer 80 exclusively provides an insulation between the ferroelectric stack including the gate electrode 50 and the source and drain contacts. Therefore, Argos et al. disclose only one gate electrode and one gate intermediate layer.

Clearly, Argos et al. do not show "a diode structure connecting said first gate electrode to said second gate electrode", as recited in claim 1 of the instant application.

Claim 1 is, therefore, believed to be patentable over the art and since claims 3 and 8 are ultimately dependent on claim 1, they are believed to be patentable as well.

In item 7 on pages 4-5 of the above-mentioned Office action, claims 4-5 and 9 have been rejected as being unpatentable over Hsu et al. in view of Argos et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 4-5 are ultimately dependent on claim 1, they are believed to be patentable as well.

Applicants acknowledge the Examiner's statement in item 8 on page 5 of the above-mentioned Office action that claims 2, 7 and 12 would be allowable if written in independent form including all of the limitations of the base claim and any intervening claims.

Since claims 1 and 11 are believed to be patentable as discussed above and claims 2, 7 and 12 are ultimately dependent on claims 1 or 11, they are believed to be patentable in dependent form. A rewrite is therefore believed to be unnecessary at this time.

In view of the foregoing, reconsideration and allowance of claims 1-12 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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Marked-Up Version of the Amended Claims:

Claim 1(amended). A ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions, said first gate intermediate layer also extending in the direction of the line running between said source/drain regions, said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode [connected] to said second gate electrode.

Claim 8(amended). The ferroelectric transistor according to claim 1, comprising an auxiliary layer disposed between said ferroelectric [layerand] layer and said first gate electrode.

Claim 11(amended). A memory cell configuration including a plurality of memory cells, each one of said plurality of said memory cells including a ferroelectric transistor, comprising:

a semiconductor substrate having a surface and having two source/drain regions therein;

a first gate intermediate layer and a first gate electrode configured on said surface of said semiconductor substrate between said source/drain regions, said first gate intermediate layer including at least one ferroelectric layer;

a second gate intermediate layer and a second gate electrode configured between said source/drain regions and extending in a direction of a line running between said source/drain regions, said first gate intermediate layer also extending in the direction of the line running between said source/drain regions, said second gate intermediate layer including a dielectric layer; and

a diode structure connecting said first gate electrode [connected] to said second gate electrode.